PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference FP2086	**FOR FURTHER ACTION**	See Form PCT/IPEA/416
International application No. **PCT/SG2004/000006**	International filing date *(day/month/year)* 6 January 2004	Priority date *(day/month/year)* 6 January 2004

International Patent Classification (IPC) or national classification and IPC

Int. Cl. [7] H04B 1/69, H04L 27/00

Applicant

AGENCY FOR SCIENCE, TECHNOLOGY AND RESEARCH et al

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 3 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. [X] *(sent to the applicant and to the International Bureau)* a total of **10** sheets, as follows:
      - [X] sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      - [ ] sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.

   b. [ ] *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or table related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

[X]	Box No. I	Basis of the report
[ ]	Box No. II	Priority
[ ]	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
[ ]	Box No. IV	Lack of unity of invention
[X]	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
[ ]	Box No. VI	Certain documents cited
[ ]	Box No. VII	Certain defects in the international application
[ ]	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of the report
7 November 2005	2 December 2005
Name and mailing address of the IPEA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	Authorized Officer **DEREK BARNES** Telephone No. (02) 6283

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/SG2004/000006

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

☐ This report is based on translations from the original language into the following language which is the language of a translation furnished for the purposes of:

☐ international search (under Rules 12.3 and 23.1 (b))

☐ publication of the international application (under Rule 12.4)

☐ international preliminary examination (under Rules 55.2 and/or 55.3)

2. With regard to the **elements** of the international application, this report is based on (*replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report*):

☐ the international application as originally filed/furnished

☒ the description:

pages **1-10, 12-15, 17-33** as originally filed/furnished

pages **11, 11a, 16** received by this Authority on **23 November 2005** with the letter of 18 November 2005

pages received by this Authority on with the letter of

☒ the claims:

pages as originally filed/furnished

pages* as amended (together with any statement) under Article 19

pages* **34-38** received by this Authority on **23 November 2005** with the letter of 18 November 2005

pages* received by this Authority on with the letter of

☒ the drawings:

pages **2-8, 10-25** as originally filed/furnished

pages* **1, 9** received by this Authority on **23 November 2005** with the letter of 18 November 2005

pages* received by this Authority on with the letter of

☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing.

3. ☐ The amendments have resulted in the cancellation of:

☐ the description, pages

☐ the claims, Nos.

☐ the drawings, sheets/figs

☐ the sequence listing (*specify*):

☐ any table(s) related to the sequence listing (*specify*):

4. ☐ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).

☐ the description, pages

☐ the claims, Nos.

☐ the drawings, sheets/figs

☐ the sequence listing (*specify*):

☐ any table(s) related to the sequence listing (*specify*):

* *If item 4 applies, some or all of those sheets may be marked "superseded."*

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/SG2004/000006

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims **1-26**	**YES**
	Claims	**NO**
Inventive step (IS)	Claims **1-26**	**YES**
	Claims	**NO**
Industrial applicability (IA)	Claims **1-26**	**YES**
	Claims	**NO**

2. Citations and explanations (Rule 70.7)

Claims 1 to 26

The claims as amended are considered novel and inventive over the cited art since the prior art documents do not teach, either individually or in obvious combination, the following features as related to generating a UWB signal. The features being recited in independent claims 1, 7 and 17:

> "differentiating the clock signal comprises feeding the clock signal to an input of an amplifier and negatively feeding back an output of the amplifier, through a low pass filter, to the amplifier input."

The closest prior art, HYUNSEOK, K. et. Al. 'Design of CMOS Scholtz's monocycle pulse generator.' In: 2003 IEEE Conference on Ultra Wideband Systems and Technologies. New York: IEEE, 16 November 2003, pages 81-85, describes Gaussian pulse generation to obtain a monocycle pulse. The citation teaches the use of a hyperbolic function and a quadrant squarer circuit producing a square wave value for said function.

The citation does not teach or fairly suggest the use of negative feedback and low pass filtering to arrive at a UWB signal from a Gaussian pulse.

generator produces a windowing pulse, C, which turns a switch 54 on-and-off to pass signal B at appropriate moments. The resultant signal, D, is a windowed sinusoid pulse of one period which is approximately a monocycle. This method of UWB signal generation has a problem of LO signal being leaked to the output, corrupting the UWB signal.

Figure 6 shows a method of UWB Signal Generation described in "Cellonics Presentation at Ultra-Wideband Seminar", Infocomm Development Authority, Singapore, 25 February 2003, Dr. Jurianto Joe. In this method, a short pulse width 61 is fed into a nonlinear circuit based on a tunnel diode 62, which causes an oscillatory response within the pulse window. This response is also a kind of UWB signal 63. This method of UWB signal generation is also not amenable to silicon IC design as a Tunnel diode is, like SRD, a very specialised component. Quoting from Electrical Engineering Training Series by Integrated Publishing (see the web-site: www . tpub.com/content/neets/book7/26a.htm), "In a Tunnel diode, the semiconductor materials used in forming a junction are doped to the extent of 1000 impurity atoms for 10 million semiconductor atoms." However, a normal diode is lightly doped with one impurity per 10 million semiconductor atoms. Hence, a tunnel diode is a very specialised component which is expensive and not available in most foundries.

The paper by Hyunseok, K. et al "Design of CMOS Scholtz's monocycle pulse generator." and In: 2003 IEEE Conference on Ultra Wide Band Systems and Technologies, New York: IEEE, 16 November 2003 pages 81 to 85 proposes a new

Scholtz's monocycle pulse and simulated on TSMC 0.1 micrometer CMOS technology. Scholtz's monocycle pulse is achieved from second derivative of a Gaussian pulse which, in turn, is roughly achieved on a quadrant squarer circuit with hyperbolic tangent input. Then Scholtz's monocycle pulse is generated by second differential operations in passive components.

EP 1370038 discloses a signal generation method which has a Gaussian approximation. A variable (V_{in}) is provided with the wave shape presenting a succession of linear transitions between levels. Each wave transition is formed into a sliding set to obtain a corresponding wavelet.

None of the above-described methods is singularly amenable being implemented in an IC design while being risk-free from LO signal leakage and providing a sufficient power swing for antenna transmission.

Figure 12 shows a current-voltage (series-series) feedback topology equivalent to the block diagram of Figure 11.

Figure 13 is a further illustration of the current-voltage (series-series) feedback topology of Figure 12.

Figure 14 shows a hybrid-π small signal circuit

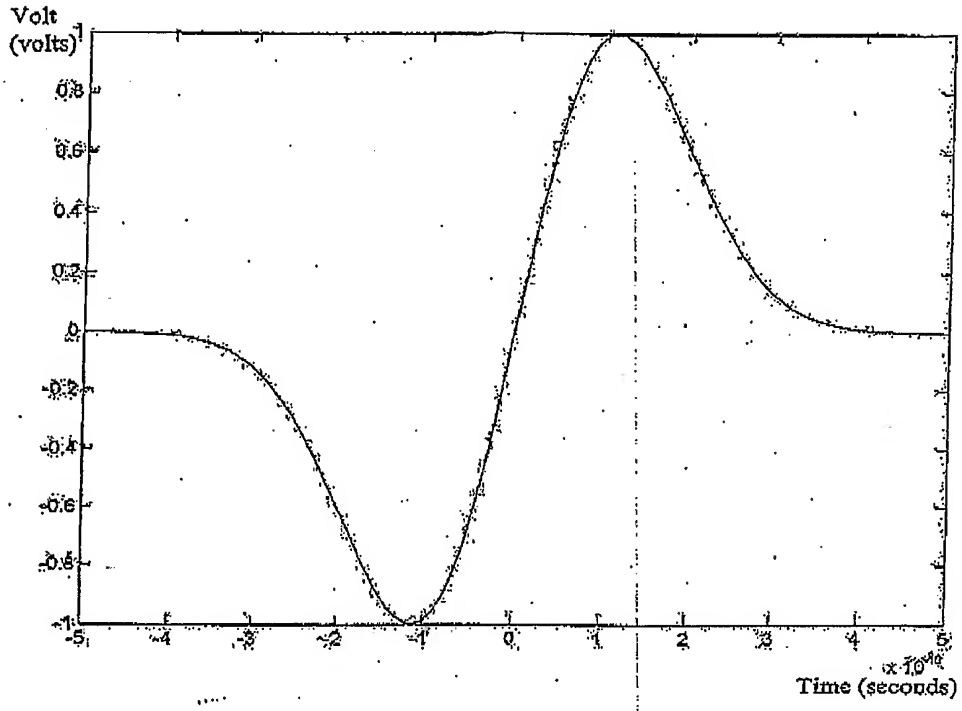
Figure 15 shows the schematics of a simple test circuit of the embodiment of Figure 12.

Figures 16a-f are graphs showing the frequency domain response of the circuit of Figure 12.

Figures 17a-f are graphs showing the time domain response of the circuit of Figure 12.

Figure 18 shows an embodiment of the UWB signal generator circuit equivalent to that of Figure 12.

Figure 19a-e illustrates the differentiating function of an embodiment of the UWB generator.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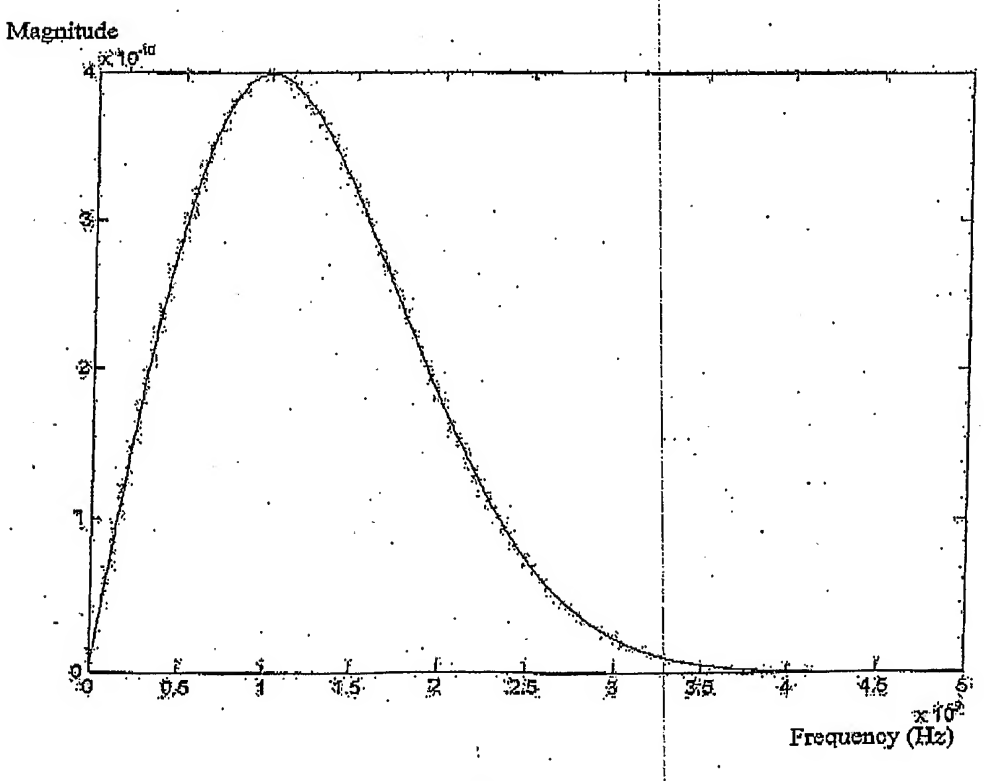
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
-5
-4
-3
-2
-1
0
1
2
3
4
5
x 10^-9
Time (seconds)

Fig 1a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0
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2.5
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3.5
4
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5
x 10^9
Frequency (Hz)

Fig 1b

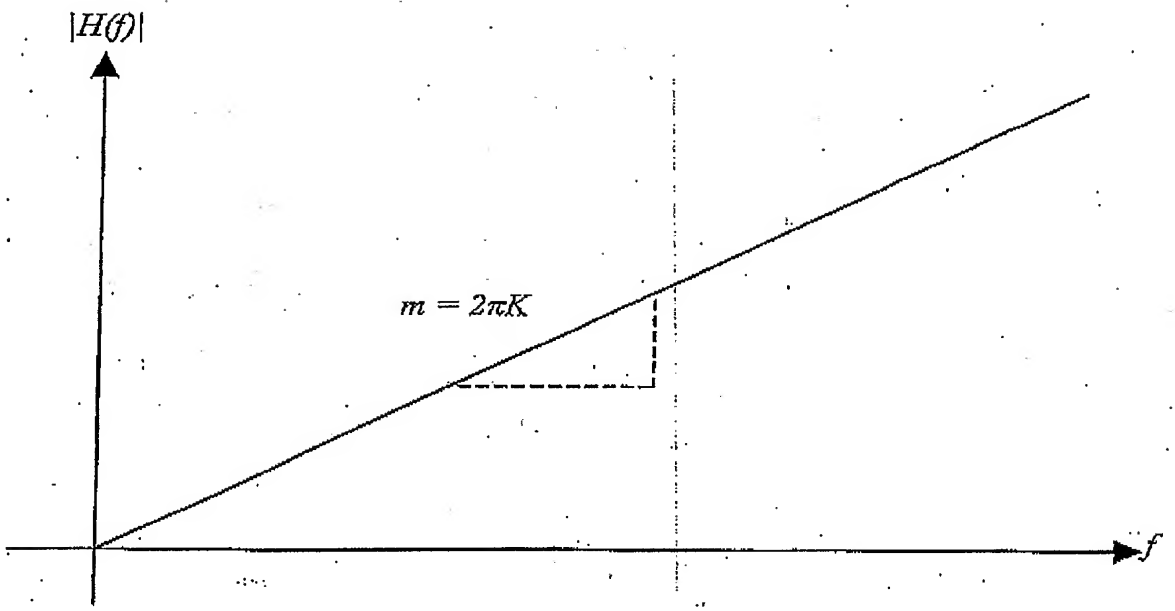

Fig 8

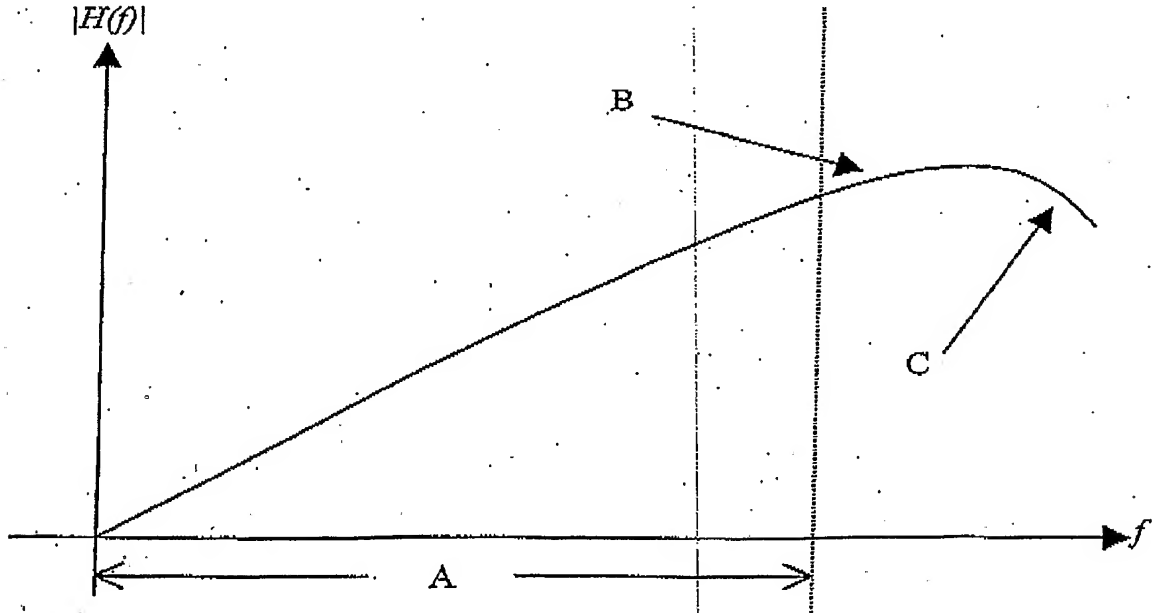

Fig 9

CLAIMS

1. A method for generating a UWB signal comprising the step of differentiating a clock signal once to obtain the UWB signal, wherein the step of differentiating the clock signal comprises feeding the clock signal to an input of an amplifier and negatively feeding back an output of the amplifier, through a low pass filter, to the amplifier input.

2. A method according to claim 1 further comprising the step of differentiating the UWB signal at least once to generate a monocyclical or a polycyclical UWB signal.

3. A method according to claim 1 further comprising the step of modulating a data signal with the UWB signal to obtain a modulated UWB signal.

4. A method according to claim 3 further comprising the step of differentiating the modulated UWB signal at least once to generate a monocyclical or a polycyclical UWB signal.

5. The method of claim 3 wherein the modulated UWB signal is amplitude-modulated.

6. The method of claim 3 wherein the modulated UWB signal is pulse-position-modulated.

7. A method for generating a UWB signal in a system comprising:

an amplifier having an input and an output;

negative feedback means;

a low-pass filtering means; and

a DC decoupling means

wherein the method comprises:

providing an output of the system to the low-pass filtering means to produce a low-pass filtered output;

feeding back, by the negative feedback means, the amplifier low-pass filtered output to the input of the amplifier;

applying the DC decoupling means to remove DC components from the amplifier output; wherein

the output of the system is an amplified differential of an input signal to the system; and

whereby a UWB pulse is produced for transmission.

8. A method according to claim 7, wherein the amplifier means comprises a biased transistor.

9. A method as claimed in claims 7 or 8 wherein the input signal is a clock signal.

10. A method as claimed in claims 7 or 8 wherein the input signal is a saw tooth signal.

11. A method as claimed in claims 7 or 8 wherein the input signal is a pulse signal.

12. A method as claimed in claims 7 or 8 wherein the system is implemented in an Integrated Circuit.

13. A method as claimed in claims 7 to 12 wherein the system comprises current-voltage topology.

14. A method as claimed in claims 7 to 12 wherein the system comprises voltage-voltage topology.

15. A method as claimed in claims 7 to 12 wherein the system comprises voltage-current topology.

16. A method as claimed in claims 7 to 12 wherein the system comprises current-current topology.

17. A system comprising:

an amplifier having an input and an output;

negative feedback means;

a low-pass filtering means;

a DC decoupling means

the amplifier providing an output of the system to the low-pass filtering means to produce a low-pass filtered output;

the negative feedback means feeding back the low-pass filtered output of the amplifier is negatively fedback to the input means of the amplifier;

the DC decoupling means removing DC components from the amplifier output; wherein

the output of the system is an amplified differential of an input signal to the system; and

whereby

a UWB pulse is produced for transmission.

18. A system as claimed in claim 17 wherein the amplifier means comprises of a biased transistor.

19. A system as claimed in claims 17 or 18 wherein the input signal is a clock signal.

20. A system as claimed in claims 17 or 18 wherein the input signal is a saw tooth signal.

21. A system as claimed in claims 17 or 18 wherein the input signal is a pulse signal.

22. A system as claimed in claims 17 or 18 wherein the system is implemented in an Integrated Circuit.

23. A system as claimed in claims 17 to 22 wherein the system comprises current-voltage topology.

24. A system as claimed in claims 17 to 22 wherein the system comprises voltage-voltage topology.

25. A system as claimed in claims 17 to 22 wherein the system comprises voltage-current topology.

26. A system as claimed in claims 17 to 22 wherein the system comprises current-current topology.